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United States Patent [19]

Cova

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[45] Date of Patent: Oct. 31, 2000

[54] **PREDISTORTION IN A LINEAR TRANSMITTER USING ORTHOGONAL KERNELS**

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[73] Assignee: **Glenayre Electronics, Inc.**, Charlotte, N.C.

[21] Appl. No.: **08/965,097**

[22] Filed: **Nov. 6, 1997**

Related U.S. Application Data

[63] Continuation-in-part of application No. 08/850,940, May 5, 1997, Pat. No. 5,923,712.

[51] **Int. Cl.**[7] **H03F 1/26**; H04L 25/49

[52] **U.S. Cl.** **375/297**; 375/296; 375/285; 455/126; 330/149; 332/162

[58] **Field of Search** 375/297, 296, 375/285, 284; 455/126, 63; 330/149; 332/103, 162, 160, 159, 124, 123

[56] **References Cited**

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5,867,065	2/1999	Leyendecker	330/149
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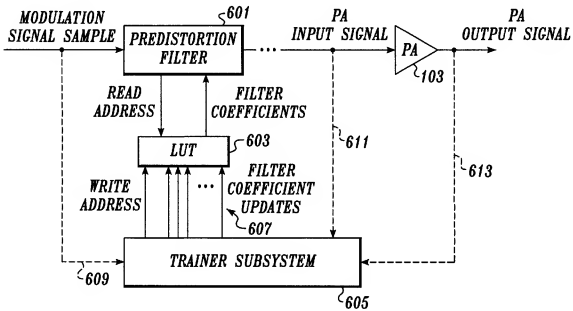
Primary Examiner—Young T. Tse

Attorney, Agent, or Firm—Christensen O'Connor Johnson Kindness PLLC

[57] **ABSTRACT**

A system for linearly transmitting an amplified output signal using predistortion is disclosed. The system uses a straight inverse modeling scheme with orthogonal predictor variables to more easily and accurately determine the inverse of the distortion caused by a power amplifier of a RF transmitter. The direct inverse modeling scheme of the present invention indexes the LUT using the modulated input signals instead of the potentially noisier output signals, which helps to increase the accuracy of the predistortion. The predistorter system stores complex coefficients in the LUT, which are then used as the tap weights of a non-linear digital filter implementing the predistorter. Finally, the trainer uses a modified version of the power amplifier output signal which results in better predistortion performance. The modified power amplifier output signal has the in-band distortion removed from the power amplifier output signal.

19 Claims, 12 Drawing Sheets



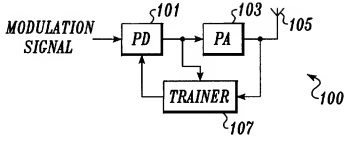


Fig. 1.
(PRIOR ART)

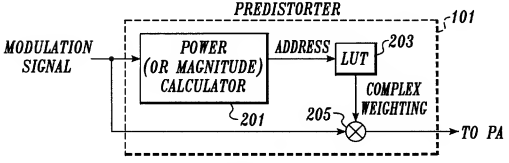


Fig. 2.
(PRIOR ART)

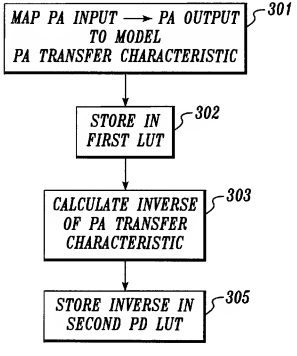


Fig. 3.
(PRIOR ART)

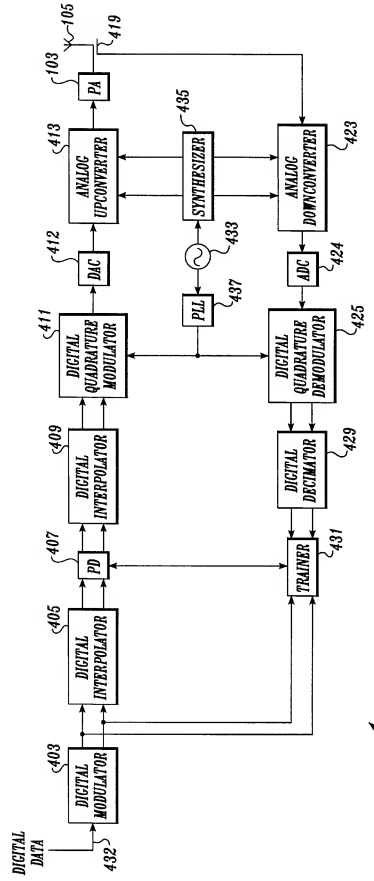

DIGITAL DATA
432
DIGITAL MODULATOR
403
DIGITAL INTERPOLATOR
405
PD
407
DIGITAL INTERPOLATOR
409
DIGITAL QUADRATURE MODULATOR
411
DAC
412
ANALOG UPCONVERTER
413
PA
103
105
419
SYNTHESIZER
435
433
PLL
437
ANALOG DOWNCONVERTER
423
ADC
424
DIGITAL QUADRATURE DEMODULATOR
425
DIGITAL DECIMATOR
429
TRAINER
431
400

Fig. 4.

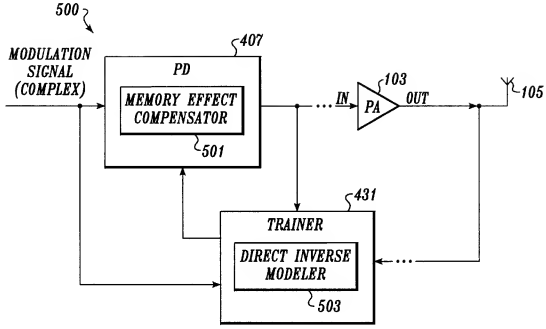
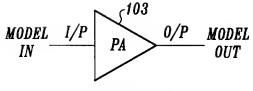
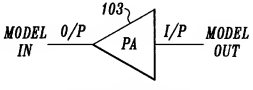


Fig. 5.



FORWARD MODEL

Fig. 5A.



DIRECT INVERSE MODEL

Fig. 5B.

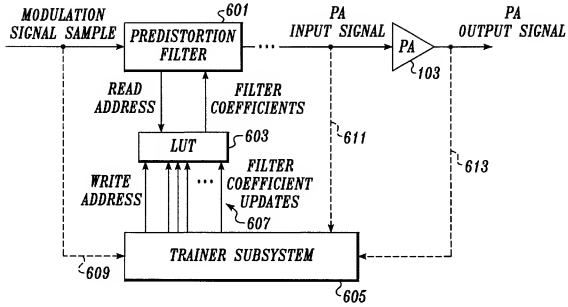

MODULATION SIGNAL SAMPLE
601
PREDISTORTION FILTER
PA INPUT SIGNAL
PA
103
PA OUTPUT SIGNAL
READ ADDRESS
FILTER COEFFICIENTS
LUT
603
611
613
WRITE ADDRESS
FILTER COEFFICIENT UPDATES
607
TRAINER SUBSYSTEM
609
605

Fig. 6.

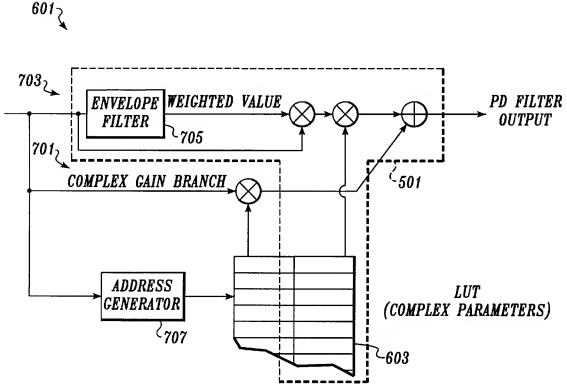

601
703
ENVELOPE FILTER
WEIGHTED VALUE
705
PD FILTER OUTPUT
701
COMPLEX GAIN BRANCH
501
ADDRESS GENERATOR
707
LUT (COMPLEX PARAMETERS)
603

Fig. 7.

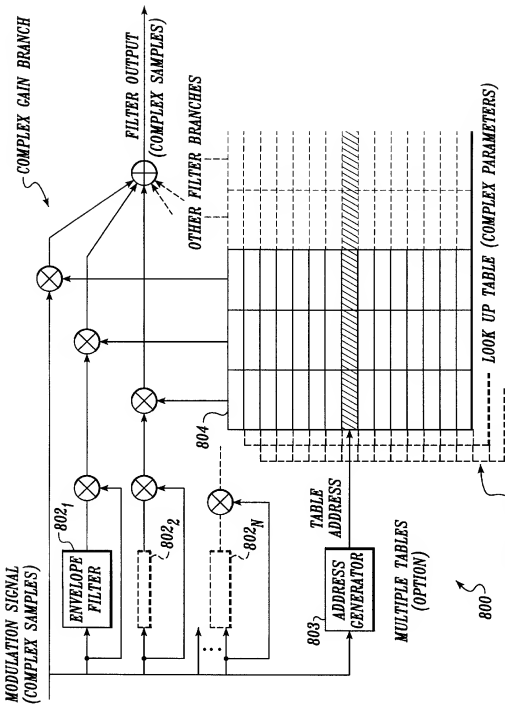

COMPLEX GAIN BRANCH
FILTER OUTPUT
(COMPLEX SAMPLES)
OTHER FILTER BRANCHES
MODULATION SIGNAL
(COMPLEX SAMPLES)
ENVELOPE FILTER
802₁
802₂
802_N
804
TABLE ADDRESS
803
ADDRESS GENERATOR
MULTIPLE TABLES (OPTION)
800
806₁–806_M
LOOK UP TABLE (COMPLEX PARAMETERS)

Fig. 8.

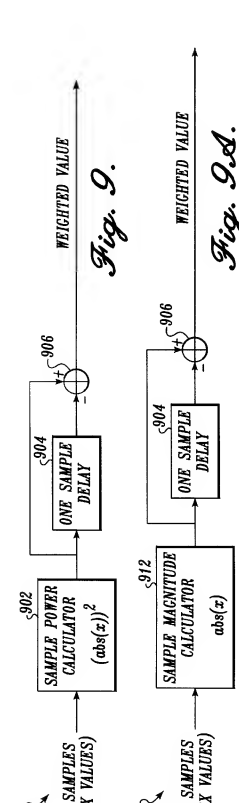


Fig. 9.

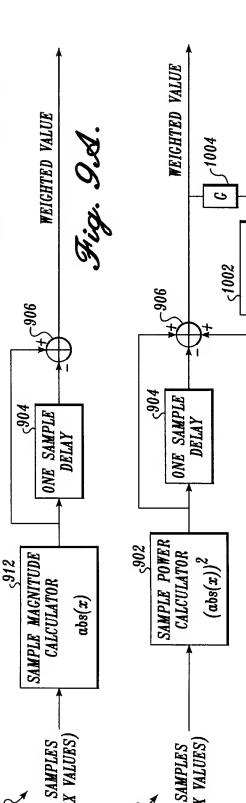


Fig. 9A.

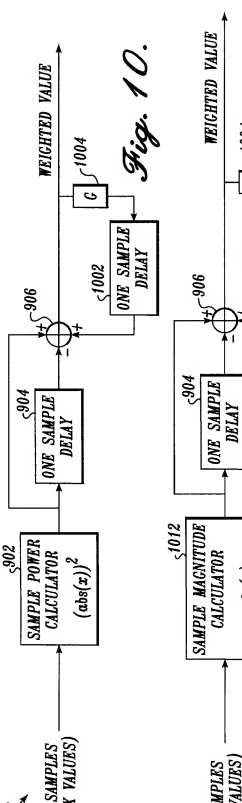


Fig. 10.

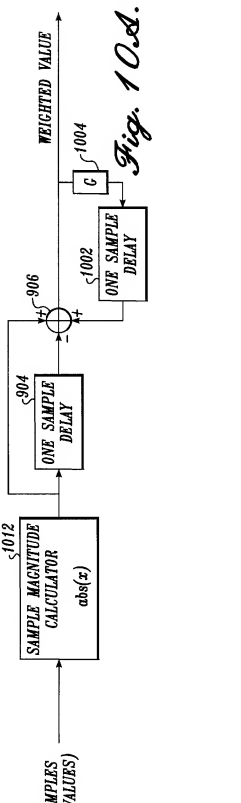


Fig. 10A.

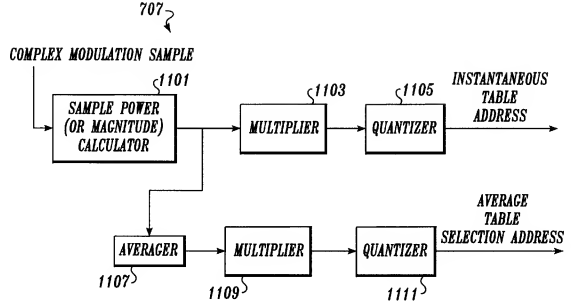

707
COMPLEX MODULATION SAMPLE
1101
SAMPLE POWER (OR MAGNITUDE) CALCULATOR
1103
MULTIPLIER
1105
QUANTIZER
INSTANTANEOUS TABLE ADDRESS
AVERAGER
1107
MULTIPLIER
1109
QUANTIZER
1111
AVERAGE TABLE SELECTION ADDRESS

Fig. 11.

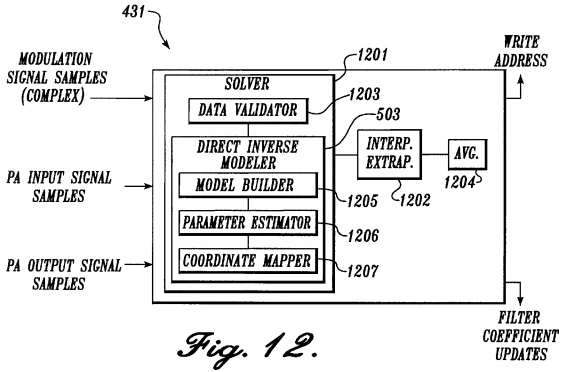

431
MODULATION SIGNAL SAMPLES (COMPLEX)
PA INPUT SIGNAL SAMPLES
PA OUTPUT SIGNAL SAMPLES
1201
SOLVER
DATA VALIDATOR
1203
503
DIRECT INVERSE MODELER
MODEL BUILDER
1205
PARAMETER ESTIMATOR
1206
COORDINATE MAPPER
1207
INTERP. EXTRAP.
1202
AVG.
1204
WRITE ADDRESS
FILTER COEFFICIENT UPDATES

Fig. 12.

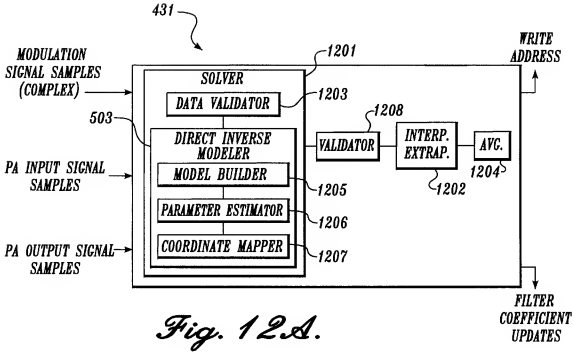


Fig. 12A.

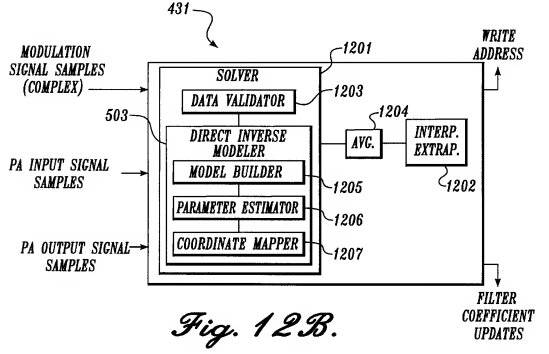


Fig. 12B.

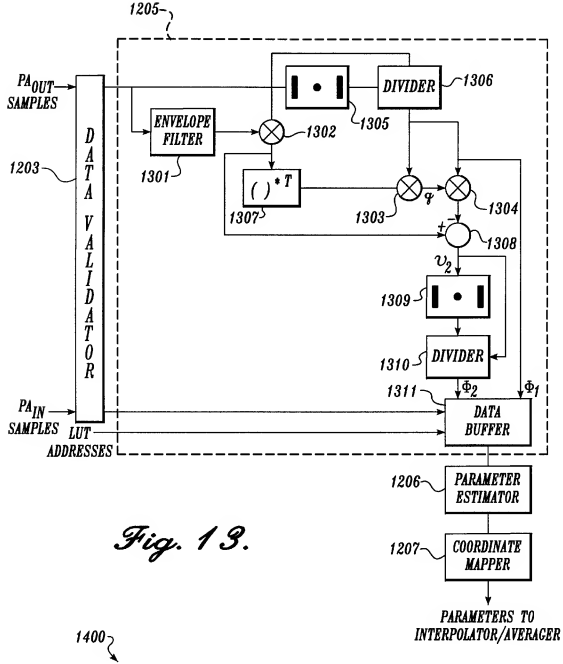

1205
PA OUT SAMPLES
DATA VALIDATOR
1203
ENVELOPE FILTER
1301
1302
1305
DIVIDER
1306
( ) * T
1307
1303
1304
1308
1309
DIVIDER
1310
1311
DATA BUFFER
PA IN SAMPLES
LUT ADDRESSES
1206
PARAMETER ESTIMATOR
1207
COORDINATE MAPPER
PARAMETERS TO INTERPOLATOR/AVERAGER

Fig. 13.

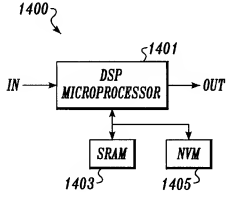

1400
1401
DSP MICROPROCESSOR
IN
OUT
SRAM
NVM
1403
1405

Fig. 14

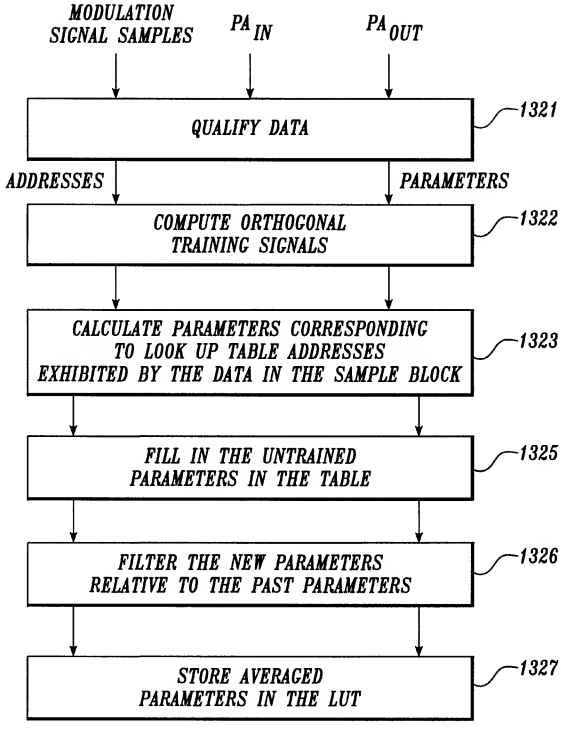

MODULATION SIGNAL SAMPLES
PA IN
PA OUT
QUALIFY DATA
1321
ADDRESSES
PARAMETERS
COMPUTE ORTHOGONAL TRAINING SIGNALS
1322
CALCULATE PARAMETERS CORRESPONDING TO LOOK UP TABLE ADDRESSES EXHIBITED BY THE DATA IN THE SAMPLE BLOCK
1323
FILL IN THE UNTRAINED PARAMETERS IN THE TABLE
1325
FILTER THE NEW PARAMETERS RELATIVE TO THE PAST PARAMETERS
1326
STORE AVERAGED PARAMETERS IN THE LUT
1327

Fig. 13A.

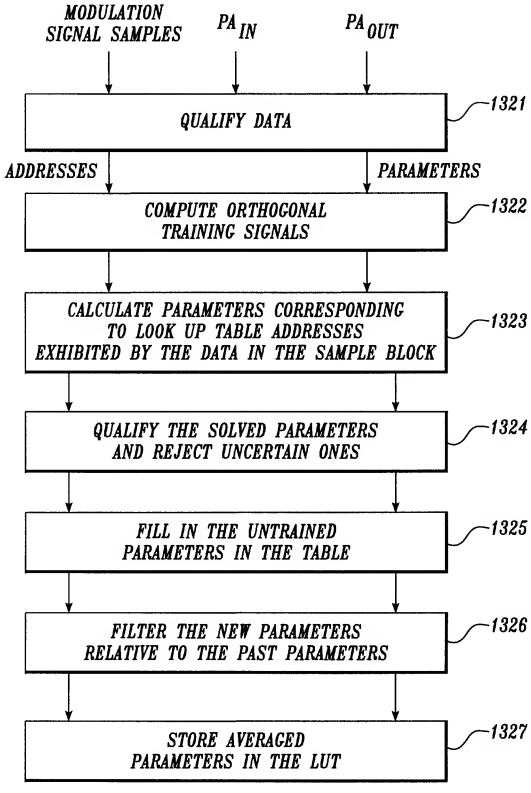

MODULATION SIGNAL SAMPLES
PA IN
PA OUT
QUALIFY DATA
1321
ADDRESSES
PARAMETERS
COMPUTE ORTHOGONAL TRAINING SIGNALS
1322
CALCULATE PARAMETERS CORRESPONDING TO LOOK UP TABLE ADDRESSES EXHIBITED BY THE DATA IN THE SAMPLE BLOCK
1323
QUALIFY THE SOLVED PARAMETERS AND REJECT UNCERTAIN ONES
1324
FILL IN THE UNTRAINED PARAMETERS IN THE TABLE
1325
FILTER THE NEW PARAMETERS RELATIVE TO THE PAST PARAMETERS
1326
STORE AVERAGED PARAMETERS IN THE LUT
1327

Fig. 13B.

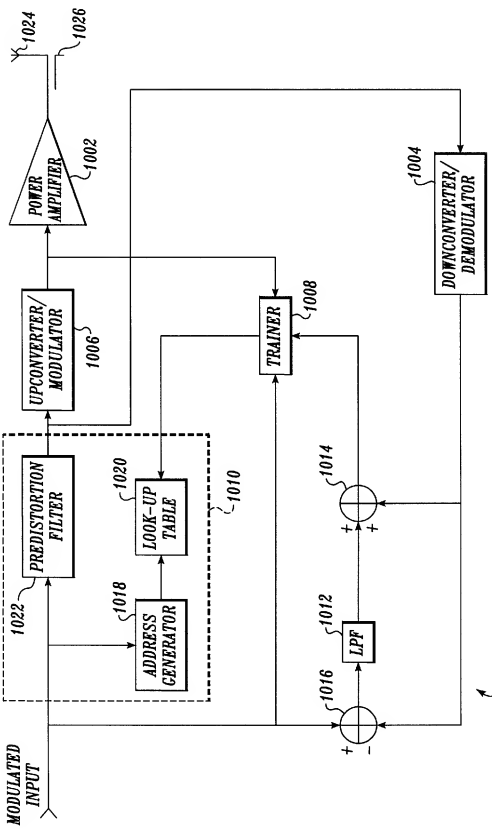

1024
1026
POWER AMPLIFIER
1002
1004
DOWNCONVERTER/ DEMODULATOR
UPCONVERTER/ MODULATOR
1006
TRAINER
1008
PREDISTORTION FILTER
1022
1020
LOOK-UP TABLE
1010
1014
1018
ADDRESS GENERATOR
1012
LPF
1016
MODULATED INPUT
1000

Fig. 15.

PREDISTORTION IN A LINEAR TRANSMITTER USING ORTHOGONAL KERNELS

RELATED APPLICATIONS

This is a continuation-in-part of 08/850,940 U.S. Pat. No. 5,923,712 entitled "Method and Apparatus for Linear Transmission by Direct Inverse Modeling," to Leyendecker et al., filed on May 5, 1997, assigned to the same assignee herein, and expressly incorporated in its entirety by reference herein, and further, this application is related to U.S. Pat. No. 5,867,065 entitled "Frequency Selective Predistortion in a Linear Transmitter" to Leyendecker et al., filed on May 7, 1997, assigned to the same assignee herein, and expressly incorporated in its entirety by reference herein.

FIELD OF THE INVENTION

The present invention relates to linear transmitters and, more particularly, to linear transmitters using predistortion.

BACKGROUND OF THE INVENTION

It is well-known that the power amplification stages of typical radio frequency (RF) broadcast transmitters behave in a nonlinear fashion when operated near peak capacity. One simple solution to this problem is to "back off" the power amplifier and only operate the power amplifier below saturation in its linear region. However, backing off the power amplifier tends to reduce the power conversion efficiency of the power amplifier. Additionally, for a given required transmitter output power, the power amplifier used must be larger (and more expensive) than a power amplifier that can be operated at peak capacity.

Furthermore, although backing off would allow the power output of the power amplifier to behave more linearly, backing off would not alleviate the phase distortion of the power amplifier. For modulation schemes that only depend upon modulation of amplitude (such as AM), phase distortion is of relatively little concern. However, for other types of modulation schemes that rely upon both amplitude and phase modulation, phase distortion is an important concern.

An alternative solution, commonly referred to as predistortion, compensates for the distortion caused by the power amplifier by "predistorting" the signal to be amplified with the "inverse" of the transfer characteristic of the power amplifier. FIG. **1** is a simplified block diagram of an exemplary conventional predistortion subsystem **100** for use in a transmitter. A predistorter **101** is coupled to receive a modulation signal to be amplified by a power amplifier **103** and broadcast through an antenna **105**. The predistorter **101** operates on the received modulation signal to predistort the modulation signal with the calculated inverse of the transfer characteristic of the power amplifier **103**. Thus, ideally, the "predistortion" and the power amplifier distortion cancel each other out to achieve a linear amplification of the output signal. In this example, the predistortion subsystem **100** includes a trainer **107** to monitor the power amplifier input and output signals to determine the distortion caused by the power amplifier **103**, which may change over time. The trainer **107** then provides signals to update the predistorter **101** so that predistorter **101** tracks any changes in the transfer characteristic of the power amplifier **103**.

FIG. **2** is a simplified block diagram of the conventional predistorter **101** (FIG. **1**). Typical conventional predistortion schemes attempt to model the performance of the power amplifier and calculate the "inverse" of the amplifier transfer characteristic. All of the predistortion schemes known to the inventors of the present invention attempt to model the power amplifier performance as a function of the instantaneous power or magnitude envelope of the input signal to the power amplifier. Accordingly, these conventional predistortion schemes predistort the input signal as a function of the power or magnitude of the signal to be amplified. For example, U.S. Pat. No. 4,291,277 issued to Davis et al. and U.S. Pat. No. 5,049,832 issued to Cavers disclose such a scheme. Thus, in this scheme, the predistorter **101** includes a power calculator **201** for calculating the instantaneous power or magnitude of the received modulation signal. The calculated instantaneous power or magnitude is then used to access a look-up table (LUT) **203** that stores a corresponding complex value for this particular instantaneous power or magnitude. This complex value approximates the local inverse of the transfer characteristic of the power amplifier for this particular instantaneous power or magnitude of the modulation signal. The LUT **203** can be periodically updated by the trainer **107** (FIG. **1**) so that the complex values reflect any changes in the transfer characteristic of the power amplifier **103** (FIG. **1**). The LUT **203** provides this complex value to a multiplier **205**, which multiplies the modulation signal with this complex value to predistort the modulation signal. Thus, when the predistorted modulation signal is subsequently amplified by the power amplifier, the predistortion cancels to some extent the distortion caused by the power amplifier.

Although these conventional predistortion schemes represent an improvement over earlier schemes to reduce power amplifier distortion, the inventors of the present invention have observed that modeling the power amplifier transfer characteristic using only the instantaneous power or magnitude does not completely accurately predict the distortion caused by the power amplifier. Consequently, predistortion schemes based on such models cannot completely correct the distortion caused by the power amplifier.

FIG. **3** is a flow chart illustrative of a conventional process of calculating the complex values that are stored in the LUT **203** (FIG. **2**). In a step **301**, the trainer **107** (FIG. **1**) determines the instantaneous magnitude and phase of the input signal to the power amplifier **103** (FIG. **1**) and the instantaneous magnitude and phase of the amplified (and distorted) output signal. The trainer **107** typically stores these values in a LUT (not shown) within the trainer and, thus, can directly model the transfer characteristics of the power amplifier **103**. In step **302**, these characteristics are stored in a first lookup table (LUT). This first trainer LUT is indexed using the actual amplifier output power or magnitude. Then in a next step **303**, the trainer **107** calculates the mathematical "inverse" of the transfer characteristic of the power amplifier. This step is generally computationally intensive, thereby undesirably increasing the complexity of the hardware and software of the trainer **107** and consuming processing time and power. In addition, because the trainer LUT is indexed by actual amplifier output power or magnitude, addressing errors may occur because the amplifier output signal is potentially noisy. Then in a step **305**, the trainer stores the calculated inverse in the second LUT **203** of the predistorter **101**.

In view of the above shortcomings of conventional predistortion schemes, there is a need for a predistortion system that will compensate for power amplifier distortion more accurately than the conventional predistortion systems that are based on instantaneous envelope power or magnitude. There is also a need for a less complex and more accurate scheme to provide the inverse of the power amplifier transfer characteristic.

SUMMARY OF THE INVENTION

In accordance with the present invention, a system for linearly transmitting an amplified output signal using predistortion is provided. In one embodiment adapted for use with digital input data, the system uses a straight inverse modeling scheme to more easily and accurately determine the inverse of the distortion caused by a power amplifier of a RF transmitter. In this embodiment, the "inverse" of the power amplifier is directly modeled by considering the power amplifier as a signal processing block with the input and output ports reversed. More specifically, the output signal of the power amplifier is considered the input signal of the "inverse" power amplifier model and, correspondingly, the modulated input signal of the power amplifier is considered the output signal of the "inverse" power amplifier model. As a result, the computationally intensive inversion required by the conventional schemes is avoided, which serves to free up resources and reduce processing time and power consumption. Further, unlike the conventional inverse modeling schemes, the direct inverse modeling scheme of the present invention indexes the LUT using the modulated input signals instead of the potentially noisier output signals, which helps to increase the accuracy of the predistortion. In addition, in one embodiment, the predistorter system stores complex coefficients in the LUT, which are then used as the tap weights of a digital filter implementing the predistorter.

In accordance with other aspects of the present invention, the direct inverse modeling scheme of this invention uses orthogonal signals for training. This has been found to significantly improve predistortion performance as compared to the direct, inverse modeling method described in U.S. Pat. No. 5,923,732 entitled "Method and Apparatus for Linear Transmission by Direct Inverse Modeling."

In accordance with still other aspects of the present invention, the trainer uses a modified version of the power amplifier output signal. The modified power amplifier output signal has the in-band distortion removed from the power amplifier output signal. As a result of this pre-conditioning of the power amplifier output signal, significant reductions in the nonlinear distortion of the power amplifier can be achieved.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

FIG. **1** is a block diagram of a conventional predistortion system;

FIG. **2** is a block diagram of a conventional predistorter as depicted in FIG. **1**;

FIG. **3** is a flow diagram of a conventional process to calculate the complex values of the predistorter depicted in FIG. **2**;

FIG. **4** is a block diagram of a transmitter using a predistortion system according to one embodiment of the present invention;

FIG. **5** is a block diagram of a predistortion system according to one embodiment of the present invention;

FIG. **5**A and FIG. **5**B are block diagrams illustrating direct inverse modeling according to one embodiment of the present invention;

FIG. **6** is a more detailed block diagram of the predistortion system depicted in FIG. **5**;

FIG. **7** is a block diagram of a predistortion filter according to one embodiment of the present invention;

FIG. **8** is block diagram of a predistortion filter according to a second embodiment of the present invention;

FIG. **9** is a block diagram of an envelope filter according to one embodiment of the present invention;

FIG. **9**A is a block diagram of an envelope filter according to a second embodiment of the present invention;

FIG. **10** is a block diagram of an envelope filter according to a third embodiment of the present invention;

FIG. **10**A is a block diagram of an envelope filter according to a fourth embodiment of the present invention;

FIG. **11** is a functional block diagram of a look-up table address generator according to one embodiment of the present invention;

FIGS. **12**, **12**A and **12**B are functional block diagrams of a trainer according to different embodiments of the present invention;

FIG. **13** is a functional block diagram of the solver depicted in the trainer of FIG. **12**, according to one embodiment of the present invention;

FIGS. **13**A and **13**B are flow diagrams illustrating the operation of the solver according to two embodiments of the present invention; and

FIG. **14** is a block diagram of digital signal processing circuit for implementing a predistorter and trainer, according to one embodiment of the present invention; and

FIG. **15** is a block diagram of an alternative embodiment of the present invention.

DETAILED DESCRIPTION

FIG. **4** is a functional block diagram of a linear transmitter **400** using a predistortion system according to one embodiment of the present invention. This embodiment of the transmitter is substantially similar to the transmitter described in U.S. Pat. No. 5,732,333 entitled "Linear Transmitter Using Predistortion", which is commonly assigned to the assignee of the present invention and incorporated herein by reference. In a preferred embodiment, the linear transmitter **400** is adapted for use as a paging transmitter in a paging system, although it can be used in any radio frequency (RF) application.

The transmitter **400**, in the forward signal processing path, includes a modulator **403**, a predistorter **407**, a digital quadrature modulator **411**, a digital-to-analog converter **412**, an analog upconverter **413**, the power amplifier **103** and the transmitting antenna **105**. A feedback loop of the transmitter **400** includes a directional coupler **419** (between the power amplifier **103** and the antenna **105**), an analog downconverter **423**, an analog-to-digital converter **424**, a digital quadrature demodulator **425**, and a trainer **431**. The trainer **431** is coupled to receive the output signals of the digital modulator **403** and interact with the predistorter **407**. In other embodiments, additional power amplifiers may be connected in parallel with the power amplifier **103** to increase the gain of the transmitter **400**.

Digital data that is to be broadcast by the transmitter **400** is provided to the modulator **403**, as represented by an arrow **432**. The digital data may be provided by any source. In the preferred embodiment, the digital data received by the modulator **403** is provided from a transmitter controller (not shown) of the paging system. The transmitter controller receives data over a link channel from a paging terminal and formulates the data for transmission. The details of the

construction of a transmitter controller, and indeed an entire paging system, can be found in U.S. Pat. No. 5,481,258 to Fawcett et al., U.S. Pat. No. 5,365,569 to Witsaman et al. and U.S. Pat. No. 5,416,808 to Witsaman et al., commonly assigned to the assignee of the present invention and incorporated herein by reference.

In a preferred embodiment, the data is a series of digital symbols, with each symbol representing a predetermined number of bits. The number of bits per symbol is dependent upon the particular modulation scheme being transmitted by the transmitter **400**. Modulation formats in typical conventional paging data systems include, for example, two or four tone frequency shift keying (FSK) modulation, continuous phase FSK (CPFSK), 43K75B8E formal modulation (a type of amplitude modulation developed by Motorola) and quadrature amplitude modulation (QAM). QAM formats include, for example, an eight level QAM scheme that would have a three-bit symbol. Similarly, a sixteen level QAM scheme would have four bits per symbol. It will be appreciated that for a three-bit symbol, there are eight possible symbols. Likewise, for a four-bit symbol, there are sixteen possible symbols.

The modulator **403** correlates each particular symbol with predetermined in-phase and quadrature output signals. Thus, for each unique symbol, a different combination of in-phase and quadrature component signals for the base band signal is output by the modulator. In a preferred embodiment, the modulator **403** includes a Texas Instruments TMS320C44 digital signal processor (DSP) microprocessor that is programmed to perform the in-phase and quadrature modulation on the symbols.

Additionally, as each symbol is processed, the modulator **403** does not "instantaneously" transition from one symbol to another. Such an instantaneous change in in-phase and quadrature output signals would result in high frequency harmonics in the system. Instead, by means of digital filtering, a smooth transition between symbols (and therefore in-phase and quadrature output signals) is achieved. One embodiment of this technique which is applicable to an FSK system is disclosed in more detail in U.S. Pat. No. 5,418,818 to Marchetto et al., assigned to the same assignee as the present invention and incorporated herein by reference.

Next, the in-phase and quadrature component signals output by the modulator **403** are input into the predistorter **407**. The predistorter **407** is operative to modify the in-phase and quadrature component signals output from the modulator **403** so as to compensate for any distortion that takes place in the power amplifier **103**. In accordance with the present invention, the predistorter uses a predistortion scheme that is dependent not only on the instantaneous power or magnitude envelope of the sample, but also on the power or magnitude envelope of the previous samples. By taking into account the power or magnitude envelope of previous samples, the effect of the trajectory leading to the current sample's power or magnitude envelope is also compensated for in the predistortion of the current sample, improving the linearity of the power amplifier **103**. This predistortion scheme is described further below in conjunction with FIGS. **5**–**13**B.

The output signals of the predistorter **407** are then provided to the digital quadrature modulator **411**. The digital quadrature modulator **411** converts the in-phase and quadrature component signals into a single real digital signal. The real digital signal from the digital quadrature modulator **411** is received by a D-A converter **412** that converts the real digital signal to an analog signal, producing an intermediate frequency output signal. For example, the intermediate frequency is approximately 5.6 MHz in a representative embodiment. Because a single D-A converter is used, the distortion caused by the relative delay and amplitude differences introduced in those conventional systems that use separate D-A for in-phase and quadrature signals is substantially eliminated in the transmitter **400**.

The intermediate frequency output signal from the D-A converter **412** is provided to the analog upconverter **413**, which converts the intermediate frequency signal to a broadcast frequency signal having a frequency within a frequency band of the paging system. For example, the broadcast frequency is approximately 940 MHz in a representative embodiment. The analog upconverter **413** can be any suitable conventional upconverter such as, for example, a mixer receiving a local oscillator signal.

The power amplifier **103** receives the broadcast frequency signal from the analog upconverter **413**, amplifies the signal, and provides the amplified signal to the transmitting antenna **105** for transmission. In this embodiment, the power amplifier **103** is substantially similar to the power amplifier disclosed in U.S. Pat. No. 5,694,085 entitled "High-Power Amplifier Using Parallel Transistors", assigned to the same assignee as the present invention and incorporated herein by reference. Of course, any suitable power amplifier can be used in other embodiments.

In order to aid in the accurate predistortion of the signal, the feedback loop monitors the amplified signal from the power amplifier **103**. The coupler **419** is a conventional directional coupler positioned relatively close to the antenna **105** and is operative to direct a relatively small portion of the output signal from the power amplifier **103** to the analog downconverter **423**.

The analog downconverter **423** operates in an opposite manner to the analog upconverter **413**. In particular, the analog downconverter **423** lowers the frequency of the receive signal outputted by power amplifier **103** to an intermediate frequency. In a preferred embodiment, this intermediate frequency is substantially the same as the intermediate frequency used in the forward signal processing path. Within the analog downconverter **423**, there is a series of filtering, amplification, and mixing with local oscillator signals processes to generate the intermediate frequency signal, as described in the aforementioned U.S. Pat. No. 5,732,333.

Next, the intermediate frequency signal is converted from an analog intermediate frequency signal into a digital signal. This is accomplished by using a conventional A-D converter **424** such as, for example, an Analog Devices AD9026, which samples the intermediate frequency signal and outputs a digital signal representing the sampled intermediate frequency signal. The digital quadrature demodulator **425** performs a digital quadrature demodulation of the digital signals and outputs the in-phase component signal and the quadrature component signal.

The trainer **431** receives the output signals of the digital quadrature demodulator **425**. The trainer **431** also periodically receives the output signals from the modulator **403** and the predistorter **407**, as described below in conjunction with FIG. **6**. Thus, ideally, the trainer **431** receives the equivalent of the exact modulated signal that was intended to be sent (the output signals of the modulator **403**) and the signal that was actually transmitted (the output signals of the digital quadrature demodulator **425**). This scheme enables the predistorter **407** to associate the distorted output sample to its

corresponding input sample so that the predistorter **407** can more accurately compensate for the distortion caused by the power amplifier **103**. Typically, the trainer provides one or more "trainer" signals to the predistorter to update the predistorter's response to the in-phase and quadrature signals input to the predistorter as the power amplifier's response changes due to temperature, age, etc.

In addition, the trainer monitors the actual data or voice signals being transmitted to implement the predistortion scheme, as opposed to special sequences (i.e., not normal data or voice signals) as required by some conventional systems. Thus, normal data or voice transmissions need not be interrupted to transmit special data sequences to update the predistorter as in these conventional systems.

In a further refinement, the transmitter **400** may include digital interpolators **405** and **409**, and a digital decimator **429**. The digital interpolator **405** is connected between the modulator **403** and the predistorter **407**, the digital interpolator **409** is connected between the predistorter **407** and the digital quadrature modulator **411**, and the digital decimator **429** is connected between the digital quadrature demodulator **425** and the trainer **431**. This circuitry provides further upconversion in the forward signal processing path and corresponding downconversion in the feedback path.

In addition, the transmitter **400** includes a synthesizer **435** connected to the analog upconverter **413** and the analog downconverter **423**, a phase locked loop (PLL) **437** connected to the digital quadrature modulator **411**. An ovenized reference oscillator **433** is connected to both the synthesizer **435** and the PLL **437**. This timing circuitry ensures that the modulation, upconversion, downconversion and demodulation are accurately synchronized.

In this embodiment, the output signals of the modulator **403** are the in-phase and quadrature component signals sampled at 80,000 samples per second (80 ksps). The in-phase and quadrature component signals output by the modulator **403** are received by the digital interpolator **405**. The digital interpolator **405** operates to increase the effective sampling rate of the received signals by means of digital interpolation. In a preferred embodiment, the digital interpolator **405** outputs the in-phase and quadrature component signals at a rate of approximately 800 ksps and is implemented with a DSP module having a TMS320C44 DSP microprocessor and associated memory, as described below in conjunction with FIG. **14**.

The signals output by the interpolator **405** are received by the predistorter **407**. The predistorter **407**, as previously described, predistorts the received in-phase and quadrature component signals to compensate for the distortion of the power amplifier **103**. The predistorted 800 ksps component signals from the predistorter **407** are received by the digital interpolator **409**. The digital interpolator **409** operates in a fashion similar to the interpolator **405** to increase the effective sampling rate. Specifically, both the in-phase and quadrature component signals are first upconverted in a first step by a factor of two. Thus, after this first conversion, the effective sampling rate of the component signals is approximately 1.6 Msps. The signals are then upconverted by another factor of two, resulting in an effective rate of approximately 3.2 Msps. Next, these two 3.2 Msps signals are passed to a further interpolator which upconverts them by a factor of seven to approximately 22.4 Msps. Thus, the output signals of the digital interpolator **409** are in-phase and quadrature component signals that have been sampled at 22.4 Msps. The interpolation stages include digital filtering of the base band signals. The implementation of the digital interpolator **409** is described in more detail in the aforementioned U.S. Pat. No. 5,732,333.

The digital quadrature modulator **411** receives the output signals of the digital interpolator **409** and modulates them as previously described using a digital quadrature modulation scheme. In this embodiment, the digital quadrature modulator **411** uses a digital equivalent of a conventional double balanced modulation scheme in conjunction with a 5.6 MHz carrier signal derived from a 22.4 MHz signal provided by the PLL **437**. The real digital modulated output signal is then converted to an analog signal by the D-A converter **412**. As a result, the D-A converter **412** outputs a 5.6 MHz analog intermediate frequency signal to the analog upconverter **413**.

The analog upconverter **413** receives two local oscillator signals provided by the synthesizer **435**. In a preferred embodiment in which the broadcast frequency is 940 MHz, the two frequencies provided by the synthesizer **435** are a 36.9 MHz local oscillator signal and a 897.5 MHz local oscillator signal. The analog upconverter **413** receives the local oscillator signals for mixing with the 5.6 MHz intermediate frequency signal in a conventional two-stage mixing scheme. In the first stage of the upconversion, the intermediate signal is mixed with the 36.9 MHz local oscillator signal, and the upper side band of the resulting 42.5 MHz signal is amplified and bandpass filtered before being mixed with the 897.5 MHz local oscillator signal. The resulting upper side band at 940 MHz is bandpass filtered and provided to the power amplifier **103**. It will be appreciated by those skilled in the art of linear RF transmitters that to change the frequency of transmission of the transmitter **400**, the local oscillator frequencies generated by the synthesizer **435** can be changed. The 940 MHz signal is then amplified by the power amplifier **103** and broadcast through antenna **105** as previously described for transmitter **400**.

In a preferred embodiment, the synthesizer **435** is a Phillips SA7025 synthesizer chip. As noted above, the synthesizer **435** controls the variable local oscillator signal for precisely determining the transmit frequency of the signal. The synthesizer **435** uses a reference oscillator **433** that, in a preferred embodiment, is a stable reference at 10 MHz. In this preferred embodiment, this 10 MHz stable reference is obtained from the transmitter controller of a paging base station.

The 940 MHz receive signal from the coupler **419** is provided to the analog downconverter **423**, converted to the intermediate frequency of 5.6 MHz, and received by the digital quadrature demodulator **425**. The digital quadrature demodulator **425** operates to generate in-phase and quadrature component signals at 22.4 Msps. In a preferred embodiment, the digital quadrature demodulator is implemented using a Xilinx 4003 field programmable gate array (FPGA) that has been configured to perform the digital quadrature demodulation.

The digital decimator **429** receives the output signals of the digital quadrature demodulator **425** and performs a decimation by a factor of twenty-eight to produce 800 ksps complex base band signals. The downconversion is performed, in a preferred embodiment, by two Harris HSP43220 decimating filter chips programmed to decimate by twenty-eight and to filter the base band signals.

The 800 ksps complex base band signals are received by the trainer **431**. As previously described, the trainer analyzes the receive signals and the signals from the modulator **403** to control the predistorter **407** to properly compensate for the distortion caused by the power amplifier **103**.

Another important feature of the present invention is that all of the processing done by each of the components of FIG.

4 is keyed off synchronous clock signals. By utilizing the same clocking in the demodulation scheme of components **424–429** as is used in the modulation scheme of components **403–412** and trainer **429**, it is possible to monitor the transmitted signal quality on each digital sample. The modulation and demodulation are phase locked to one another with adjustment only needed for the delay through the analog and digital stages, including the power amplifier **103**.

FIG. **5** is a functional block diagram of a predistortion system **500** according to one embodiment of the present invention, with the intervening circuitry omitted for clarity. The predistortion system **500** includes the predistorter **407**, the power amplifier **103** and the trainer **431**. In addition, the predistorter **407** and trainer **431** respectively include a memory effect compensator **501** (described further below in conjunction with FIGS. **6–8**) and a direct inverse modeller **503** (described further below in conjunction with FIGS. **5A** and **5B**).

As described above in conjunction with FIG. **4**, the predistorter **407** receives digital input samples and modifies them with, ideally, the inverse of the transfer characteristic of the power amplifier **103**. In particular, the predistorter **407** determines the instantaneous power or magnitude envelope of the current sample, with the predistortion being determined as a function of this instantaneous value. However, unlike other predistortion systems, the memory effect compensator **501** of the predistorter **407** takes into account the power or magnitude envelope of one or more previous samples. More specifically, the inventors of the present invention have observed that modeling the power amplifier transfer characteristic using only the instantaneous power or magnitude does not completely accurately predict the distortion caused by the power amplifier **103**. Further, the inventors of the present invention have observed that the power amplifier's transfer characteristic also depends on past power or magnitude envelopes, which is referred to herein as a "memory effect" of the power amplifier **103**. The memory effect of the power amplifier is related to the power or magnitude trajectory of the previous power or magnitude envelopes leading to the instantaneous power or magnitude envelope of the current sample. This memory effect is believed to be a heretofore unappreciated factor in the distortion caused by the power amplifier. By determining the predistortion for each sample as a function of both the instantaneous power or magnitude envelope and past power or magnitude envelopes, the accuracy of the predistortion can be improved. Implementations of the predistorter **407** with memory effect compensator **501** are described below in conjunction with FIGS. **7** and **8**.

As described above, the trainer **431** receives the power amplifier output signals after appropriate downconversion and analog-to-digital conversion and determines the inverse of the power amplifier transfer characteristic. The trainer **431** also receives the digital sample of the modulation signal. Because the timing and sampling is synchronized, the trainer **431** matches (by taking into account the delay through the intervening circuitry) the input digital sample with the corresponding sample of the power amplifier output signal. Thus, the trainer **431** models the inverse of the power amplifier transfer characteristic on a sample-by-sample basis. The trainer **431** then "qualifies" this "inverse" data so that the trainer only trains on valid data. This qualifying process is described below in conjunction with FIGS. **13–13B**. The trainer **431** then updates the predistorter **407** with qualifying inverses of the power amplifier transfer characteristic.

In order to reduce processing time, power dissipation and hardware, the trainer **431** includes the direct inverse modeller **503**. The block diagrams of FIGS. **5A** and **5B** illustrate the concept of direct inverse modeling. The inverse of the power amplifier transfer characteristic is modeled as a non-linear "filter" with the input and output leads interchanged. That is, the output signal of the power amplifier is considered the input to the non-linear "filter", whereas the input signal of the power amplifier is considered the output of the non-linear "filter", as shown in FIG. **5A**. The complex "gain" as determined from the output lead of the power amplifier to the input lead of the power amplifier represents the "inverse" characteristic that the predistorter should multiply with the complex modulation signal sample before amplification by the power amplifier.

Consequently, instead of building a forward model of the power amplifier transfer characteristic (e.g. FIG. **5A**) and then mathematically calculating the inverse, the trainer updates the predistorter with the "output sample-to-input sample" gain and phase of the power amplifier, indexed by the instantaneous power or magnitude of the modulation signal sample. Thus, the computationally intensive mathematical inversion process is avoided, enabling the trainer to calculate the inverse characteristic of the power amplifier at a relatively high sample rate in real time. In addition, unlike the other predistortion schemes that index the inverse characteristic using the power amplifier output samples, the trainer **431** indexes the inverse characteristic using the modulation signal samples. The modulation signal samples are typically much less noisy than the power amplifier output samples, resulting in a more accurate predistortion by the predistorter **407**.

FIG. **6** is a more detailed functional block diagram of the predistortion system **500** depicted in FIG. **5**. The predistorter **407** of this embodiment is implemented with a predistortion filter **601** and a LUT **603**. The predistortion filter **601** is implemented using a digital filter circuit (see FIG. **7**), with the filter coefficients or taps of the digital filter circuit being stored in the LUT **603**. The predistortion filter **601** provides the predistortion functionality as a function of both the instantaneous power or magnitude envelope of the current modulation signal sample and the power or magnitude envelopes of previous modulation signal samples. The trainer subsystem **605** (i.e., the trainer and circuitry for sampling, downconverting and digitizing the power amplifier output signal) periodically updates the inverse characteristics of the power amplifier **103** by providing a write address and updated filter coefficients to the LUT **603**, as shown by the lines **607**. In addition, the trainer subsystem **605** periodically receives "batches" of data containing the modulation signal samples, power amplifier input signal samples and power amplifier output signal samples as indicated by the lines **609**, **611** and **613**, respectively. The trainer subsystem **605** provides the inverse characteristics of the power amplifier to the LUT **603** as described below in conjunction with FIGS. **12–13B**.

FIG. **7** is a functional block diagram of the predistortion filter **601** according to one embodiment of the present invention. The predistortion filter **601** includes a complex gain (or static) branch **701**, and a parallel weighted branch **703** that implements the functionality of the memory effect compensator **501** (FIG. **5**). The output signals of these branches are then summed to produce the filter output signal. This filter output signal is the predistorted signal serving as a basis (i.e., before upconversion and D/A conversion) for the input signal received by the power amplifier (see FIG. **4**). Because the filter output signal is digital, the filter output signals are also referred to herein as the filter output samples. In this embodiment, the predistortion filter **601** is

implemented with a TMS320C44 DSP microprocessor and associated memory (not shown) using techniques well known in the art of digital linear transmitters. The predistortion filter **601** also includes an address generator **707** that is used to generate the read addresses to access the LUT **603**. The address generator**707** is described below in conjunction with FIG. **11**.

The static branch **701** multiplies the modulation signal sample by a complex parameter from the LUT **603**. The address generator **707** uses the instantaneous power or magnitude envelope of the current modulation signal sample to generate the address of this complex parameter. The complex parameter represents part of the "inverse" characteristic to be multiplied with the current modulation signal sample.

The weighted branch **703** includes an envelope filter **705**, which generates weighted values as a function of previous power or magnitude envelope samples. The envelope filter **705** is described further below in conjunction with FIGS. **9** and **10**. In this embodiment, the envelope filter **705** generates the weighted values as a function of the current and the previous modulation signal sample, using a first order digital filter to model the memory effects of the power amplifier. The scalar weighted values are then multiplied by the complex input samples. The resulting signal is multiplied by the complex parameters stored in the LUT **603**. In this embodiment, the LUT **603** is indexed by the instantaneous power or magnitude of the modulation samples to provide the appropriate complex parameter for the weighted branch **703**, which is calculated by the address generator **707**. This first order modeling of the memory effect is relatively simple to implement while achieving accuracy which is significantly better than from complex gain alone. In other embodiments, higher order digital filters may be used to model the memory effects of the power amplifier. In addition, in other embodiments, the LUT **603** may include additional dimensions or tables that are indexed by other pertinent parameters. For example, LUT tables may be addressed by both instantaneous power or magnitude and also by an average of envelope power or magnitude of previous samples. In addition, different tables may be used for different modulation schemes or during ramp up or ramp down of power to the power amplifier. Of course, adding additional tables tends to increase the memory requirements, processing time and power dissipation of the predistortion system. However, increased DSP microprocessor and memory device performance may make these systems easier to implement in the future.

FIG. **8** is a functional block diagram of a predistortion filter **800** having additional indexes compared to the predistortion filter **601** (FIG. **7**), according to another embodiment of the present invention. In this embodiment, the predistortion filter **800** has multiple envelope filters $\mathbf{802}_1$–$\mathbf{802}_N$, an address generator **803** and a LUT **804**. The LUT **804** has a column associated with each envelope filter, which are indexed by the address generator **803** as a function of the instantaneous power or magnitude envelope of the current modulation signal sample and power or magnitude envelopes of past modulation signal samples. The address generator **803** is described further below in conjunction with FIG. **11**.

In addition, optional LUTs $\mathbf{806}_1$–$\mathbf{806}_M$ can be included to implement a multi-table predistortion filter as described above in conjunction with FIG. **7**. The predistortion filter **800** operates in a substantially similar manner as the predistortion filter **601** (FIG. **7**), with the additional envelope filters providing additional weighted branches to account for other memory effects. For example, the envelope filters $\mathbf{802}_1$–$\mathbf{802}_N$ may correspond to actual past power or magnitude envelope samples rather than the average of past power or magnitude envelope samples as in the predistortion filter **601** (FIG. **7**). The envelope filters may also correspond to different filtered averages of past sample power or magnitude.

FIG. **9** is a functional block diagram of an envelope filter **900** implemented with a finite impulse response (FIR) digital filter, according to one embodiment of the present invention. The envelope filter **900** includes a sample power calculator **902**, a delay circuit **904** and an adder **906**. The delay circuit **904** and adder **906** form a FIR digital filter. In particular, the sample power calculator **902** provides a signal representing the power of the current modulation signal sample to the delay circuit **904** and the adder **906**. The delay circuit **906** then provides the power of the previous modulation signal sample to the adder **906**, which subtracts this previous modulation sample power from the current modulation signal power to generate the output signal of the envelope filter. The sample power calculator **902** and the FIR filter are implemented by the TMS320C44 DSP microprocessor and associated memory (not shown) using techniques well known in the art of digital linear transmitters.

FIG. **9**A illustrates an envelope filter **910** similar to that in FIG. **9** but in which the sample power calculator is replaced by a sample magnitude calculator **912**.

FIG. **10** is a functional block diagram of an envelope filter **1000** implemented with an infinite impulse response (IIR) digital filter, according to another embodiment of the present invention. The envelope filter **1000** includes the sample power calculator **902**, the delay circuit **904**, the adder **906**, a second delay circuit **1002** and a gain block **1004**. The delay circuit **904**, adder **906**, delay circuit **1002** and gain block **1004** form an IIR digital filter. In particular, the sample power calculator **902** provides a signal representing the power of the current modulation signal sample to the delay circuit **904** and the adder **906**. The delay circuit **904** then provides the power of the previous modulation signal sample to the adder **906**. The adder **906** also receives a scaled version of the previous output sample of the envelope filter from the delay circuit **1002** and the gain block **1004**. To ensure stability of the IIR digital filter, the gain block **1004** scales each output sample before the output sample is stored in the delay circuit **1002**. The adder **906** then subtracts this previous modulation sample power from the sum of the current modulation signal power and the previous envelope filter output sample to generate the output signal of the envelope filter. The sample power calculator **902** and the IIR filter are implemented by the TMS320C44 DSP microprocessor and associated memory (not shown) using techniques well known in the art of digital linear transmitters.

FIGURE **10**A illustrates an envelope filter block **1010** similar to that in FIG. **10** but in which the sample power calculator is replaced by a sample magnitude calculator **1012**.

FIG. **11** is a functional block diagram of the address generator **707** of the predistortion filter **601** (FIG. **7**), according to one embodiment of the present invention. The address generator **707** has a sample power calculator **1101**, multipliers **1103** and **1109**, quantizers **1105** and **1111**, and an averager **1107**. The sample power calculator **1101** receives the current modulation signal sample and outputs a signal representing the magnitude of the instantaneous power envelope of the current modulation signal sample. Alternatively, a sample magnitude calculator may be used instead of the

sample power calculator **1101** in other embodiments in which the predistortion scheme is based on the magnitude of the modulation signal instead of power. The aforementioned TMS320C44 DSP microprocessor (not shown) implementing the predistortion filter **601** is programmed to calculate the power or magnitude from the digital modulation signal samples.

The instantaneous power or magnitude sample from the sample power (or magnitude) calculator **1101** is received by the multiplier **1103**, which then scales the instantaneous power or magnitude sample by a constant in order to match the range of table memory addresses. The scaled instantaneous power or magnitude sample is then quantized by the quantizer **1105**. This quantized value serves as the table address for the LUT **603** (FIG. **7**), which stores the values describing the complex inverse characteristic for the branches of the predistortion filter.

In addition, the instantaneous power or magnitude sample from the sample power (or magnitude) calculator **1101** is received by the averager **1107**. In this embodiment, the averager **1107** calculates the mean of the instantaneous power or magnitude samples of the current and one or more previous power or magnitude samples. This simple scheme provides a relatively good indication of the trajectory of the instantaneous power or magnitude envelope of the current power or magnitude sample without requiring a relatively large amount of processing time, memory and hardware. Of course, in other embodiments, the average may be calculated using different schemes. For example, the average may be calculated from a different number of previous power or magnitude samples, or by using a weighted averaging scheme that gives less weight for the oldest power or magnitude samples. Then, the multiplier **1109** and quantizer **1111** provide the table address for the selection of alternative tables **806**$_1$–**806**$_M$ (FIG. **8**) as described above for the multiplier **1103** and quantizer **1105**.

In a further refinement of multi-table embodiments (e.g., see LUTs **806**$_1$–**806**$_M$ in FIG. **8**), the address generator can also receive control signals from the transmitter controller (not shown) indicative of the current modulation format (e.g., FSK, QAM, etc.) and whether the transmitter is ramping up or down in power at the start or finish of a transmission. As described in conjunction with FIG. **4**, the transmitter controller provides the modulation signal samples to the modulator **403**. In light of this disclosure, those skilled in the art of digital transmitters can adapt the transmitter controller to provide these control signals without undue experimentation. In response to these control signals, the address generator then selects the LUT corresponding to the current combination of modulation format and state of the transmitter.

FIG. **12** is a functional block diagram of the trainer **431** (FIG. **5**), which includes a solver **1201**, an interpolator/extrapolator **1202**, and an averager **1204**, according to one embodiment of the present invention. The solver **1201** includes the functionalities of a data validator **1203** and the direct inverse modeler **503**. The direct inverse modeler **503** comprises the model builder **1205**, the parameter estimator **1206** and the coordinate mapper **1207**. The trainer **431**, including the solver **1201** is implemented with a TMS320C44 DSP microprocessor and associated memory.

In operation, the trainer **431** receives and stores the modulation signal samples from the transmitter controller (not shown). The trainer **431** also receives and stores from the digital decimator **429** (FIG. **4**) complex digital signals that are scaled down, downconverted and digitized samples of the power amplifier output signals. These signals are referred to herein as the PA_{out} samples.

In addition, the trainer receives and stores complex digital signal samples corresponding to the power amplifier input signals. In a preferred embodiment, the trainer **431** generates these power amplifier input signals by duplicating the predistorter functionality to generate the same input signals (prior to interpolation, upconversion and D/A conversion) that were received by the power amplifier. These signals are referred to herein as the PA_{in} samples. This embodiment is advantageously used to reduce the interconnection required to the trainer **431**. Of course, in other embodiments, the trainer **431** may have an input port coupled to the output port of the predistorter to receive the PA_{in} samples directly from the predistorter. The trainer **431** then provides the proper delays and synchronization to match the PA_{in} samples and PA_{out} samples with the originating modulation signal samples.

The solver **1201** then periodically processes a "batch" or "block" of this stored data to generate the complex parameters used to update the LUT of the predistorter. In particular, the trainer uses the instantaneous power or magnitude of the modulation signal samples to generate the write addresses of the predistorter LUT at which the trainer stores the complex inverse characteristics obtained by the direct inverse modeller **503** (i.e., indexing the LUT using the modulation signal samples). The write addresses are obtained in the same way as the read addresses as described with respect to FIG. **11**.

In one embodiment of the solver **1201**, it first performs interpolation to increase the number and time resolution of the samples used in the training. In one embodiment, this interpolation is used to achieve, in effect, a 48 megasamples/second sampling rate. This interpolation has been found to improve the linearization of the transmitter output signals. The trainer **431** then quantizes the samples into "bins" that are equal in number to the number of table addresses in the predistorter LUT. In the preferred embodiment, the data validator **1203** checks that there are enough data samples in a bin and that their distribution is statistically significant (i.e., not too much variation). If the values associated with a bin are qualified by the data validator **1203**, then the PA_{out} samples are processed by the direct inverse modeler as described below, otherwise the bin is left empty.

First, the model builder **1205** transforms the PA_{out} samples to generate training signals (which are vectors) that are orthogonal to each other. These training signals are also referred to as "predictor variables." The parameter estimator **1206** uses these orthogonal signals together with the PA_{in} samples to derive new complex parameter values for the bin. In one embodiment of the present invention, a least squares method is employed by the parameter estimator **1206** to compute complex parameters for each bin. The coordinate mapper **1207** then maps the complex parameters calculated by the parameter estimator **1206** into the signal coordinate system used in the predistortion filter **601**. The values computed by the coordinate mapper can then be used to update the predistorter LUT. In a farther refinement, each calculated parameter can be averaged or filtered with the corresponding previously trained parameters (or, alternatively, a weighted average of previously trained parameters) to generate the updated parameter. This averaging is used to smooth out changes in the parameter and to get a better parameter estimate. This value can then be used to update the predistorter LUT.

The interpolator/extrapolator **1202** then determines the parameters of the empty bins (if any) by interpolation or

extrapolation from the other surrounding bins. Then the averager **1204** averages each calculated parameter with the corresponding parameter currently stored in the predistorter LUT. When averaging a calculated parameter with the corresponding current parameter in the predistorter LUT, the trainer reads the contents of the predistorter LUT into the trainer. Similarly, when averaging a calculated parameter with a weighted average of past parameters, the trainer may include a memory array storing the running weighted average. These averaged values are then used to update the predistorter LUT. In this embodiment, the solver **1201**, validator **1203**, interpolation/extrapolation **1202** and averaging **1204** functions are implemented in the TMS320C44 DSP microprocessor and associated memory (not shown) using techniques well known in the art of digital linear transmitters. The operation of the trainer **431** is described further below in conjunction with FIGS. **13** and **13**A.

It will be appreciated that parameters stored in the predistorter's LUT will have a pair of complex values for each address, one for each column of the LUT (e.g., see LUT **603** in FIG. **7**). One of these values corresponds to the complex parameter to be multiplied with the complex gain (static) branch of the modulation signal sample, and the other value corresponds to the complex parameter to be multiplied with the weighted branch of the modulation signal sample.

FIG. **12**A is a functional block diagram of the trainer **431** (FIG. **5**), according to another embodiment of the present invention. This embodiment is substantially similar to the embodiment of FIG. **12**, except for the inclusion of the validator **1208**. This embodiment can be advantageously used to qualify the parameter estimates computed by the coordinate mapper **1207**. In the qualification process, the validator **1208** checks each parameter value to determine whether it is reliable. For instance, the validator **1208** could check the magnitude of the complex parameters for each bin comparing it to a predetermined threshold. If the magnitude of a complex parameter does not exceed the threshold, the parameter is considered reliable. Only reliable parameters are used for processing in the interpolator/extrapolator **1202** and the averager **1204**.

FIG. **12**B is a functional block diagram of yet another embodiment of the trainer **431**. This embodiment is substantially similar to the embodiment of FIG. **12** except that the averager **1204** is connected between the solver **1201** and the interpolator/extrapolator **1202**. Thus, the calculated parameters are averaged with the stored parameters before the interpolation/extrapolation process.

FIG. **13** is a functional block diagram of the solver **1201** (FIG. **12**). The solver **1201** includes the data validator **1203**, the parameter estimator **1206**, the coordinate mapper **1207** and the model builder **1205**. The model builder **1205** includes the envelope filter **1301**, multipliers **1302**, **1303** and **1304**, adder **1308**, norm calculators **1305** and **1309**, dividers **1306** and **1310**, the conjugate transposer **1307** and the data buffer **1311**. These functions are implemented in the TMS320C44 DSP microprocessor and associated memory of the trainer **431** (FIG. **7**). The solver **1201** receives the PA_{in} and PA_{out} samples formatted as column vectors, and the addresses corresponding to these samples in the predistorters LUT derived by the modulation signal samples. The PA_{in} and PA_{out} samples are qualified by the data validator **1203** which allows further processing of these signals in the solver **1201** only if the and PA_{in} and PA_{out} samples are reliable.

The envelope filter **1301** filters the PA_{in} samples and provides an output signal as a function of previous PA_{out} samples to the multiplier **1302**. In this embodiment, the envelope filter **1301** is implemented in the same manner as the envelope filter **900** (FIG. **9** or other versions depicted in FIGS. **9**A, **10** or **10**A) of the predistorter. Consequently, the memory effects of the PA_{out} samples are determined in the same manner as in the predistorter.

In the upper signal branch of solver **1201**, the PA_{out} samples are scaled in the divider **1306**. Divider **1306** divides the imaginary and real components of the PA_{out} samples by the Euclidean norm of the PA_{out} vector. The Euclidean norm of the PA_{out} vector is computed in the norm calculator **1305**. The resulting training signal Φ_1 is input into the data buffer **1311** and the multipliers **1303** and **1304**. In the second signal branch of solver **1201**, the multiplier **1302** multiplies the envelope filter output signal with the PA_{out} samples. The signal at the output of multiplier **1302** is provided to the transposer **1307** and the adder **1308**. The transposer **1307** computes the conjugate transpose of the output of multiplier **1302** to produce a row vector. The multiplier **1303** multiplies this row vector with a column vector at the output of divider **1306**, which results in the complex value g. This constant is then used in the multiplier **1304** to scale Φ_1. The signal at the output of multiplier **1304** is subtracted from the output of multiplier **1302** in the adder **1308**. The resulting column vector v_2 is normalized by the norm calculator **1309** and divider **1310** to produce a second training signal Φ_2.

As a result of the computational procedure described above, the training signals Φ_1 and Φ_2 (also known as predictor variables) are orthogonal to each other. This training technique can be used to improve the inverse PA transfer characteristic that is computed in the solver **1201**. Also, this procedure enables the trainer **431** to gather more precise and useful information out of the PA_{out} signal. Consequently, the LUT is better trained and predistortion performance is significantly improved as compared to the method described in prior U.S. Pat. No. 5,923,732 entitled "Method and Apparatus for Linear Transmission by Direct Inverse Modeling."

The orthogonal training signals Φ_1 and Φ_2 together with the PA_{in} samples and the corresponding predistorted LUT address are stored in the data buffer **1311**. The parameter estimator **1206** then accesses the data in the data buffer **1311** to calculate the values of the complex parameters for the bin. These complex parameters are processed by the coordinate mapper **1207** which maps them into the signal coordinate system used in the predistortion filter **601**. The parameter values computed by the coordinate mapper **1207** are then used as a basis for updating the predistorter LUT. The parameters are processed by the averager **1202** and the interpolator/extrapolator **1204** (FIGS. **12** and **12**B) to generate the values for updating the predistorter LUT, as described further below in conjunction with FIG. **13**A.

In an alternative embodiment, additional envelope filters, multipliers, dividers, adders and norm calculators may be included in the solver **1201** to implement other memory effect modeling algorithms. Each additional envelope filter adds an extra orthogonal training signal Φ_1. The solver **1201** would use similar algorithms as for the two-level memory effect model to process this increased amount of data with, of course, an increase in the processing time for each block of data.

FIG. **13**A is a flow diagram illustrating the process of determining complex parameters for updating the predistorter LUT, according to one embodiment of the present invention. Referring to FIGS. **12**, **13** and **13**A, the solver **1201** calculates complex "inverse" parameters corresponding to the predistorter LUT addresses, as indicated by a

block **1323** in the flow chart of FIG. **13**A. In particular, the solver **1201** receives a block of synchronized modulation signal samples, PA_{in} samples, PA_{out} samples and LUT addresses. As described above in conjunction with FIG. **12**, these samples are quantized into bins corresponding to LUT addresses. The samples may also be interpolated to increase their numbers as described in conjunction with FIG. **12**.

The solver **1201** calculates complex parameters for each bin by computing the orthogonal training signals Φ_1 and Φ_2 at step **1322** and using them to solve for the parameter estimates. A least squares technique is used for computing the parameter estimates. More specifically, for each bin, the solver **1201** solves the regression equation:

$$PA_{outk}=CG_k\cdot\Phi_{1k}+CG2_k\cdot\Phi_{2k} \quad (1)$$

where PA_{outk} denotes the set of PA_{in} samples for bin k, CG_k and $CG2_k$ are complex coefficients for bin k, and Φ_{1k} and Φ_{2k} are orthogonal training signals for bin k computed as described above in conjunction with FIG. **13**.

The values of CG_k and $CG2_k$ are calculated by the parameter estimator **1206** according to the following equations:

$$CG_k=\Phi_{1k}{}'\times PA_{outk} \quad (2)$$

$$CG2_k=\Phi_{2k}{}'\times PA_{outk} \quad (3)$$

The prime (') indicator denotes the conjugate transpose operator.

The coordinate mapper **1207** transforms CG_k and $CG2_k$ to generate values suitable for updating the predistorter LUT. This coordinate transformation is accomplished according to the following equations below:

$$CG2_{LUTk}=\frac{CG2_k}{\|v_2\|} \quad (4)$$

$$CG_{LUTk}=\frac{1}{\|PA_{out}\|}\times(CG_k-g\times CG2_{LUTk}) \quad (5)$$

In a preferred embodiment, a next step **1326** is performed in which the averager **1202** finds a weighted average of these new parameters and the current parameters. Typically, the averaging is done so that the more weight is given to the most recent parameters. These weighted averages are then used to update the predistorter LUT at step **1327**.

FIG. **13**B is a flow diagram illustrating the process of determining complex parameters for updating the predistorter LUT, according to another embodiment of the present invention. This embodiment is substantially similar to the embodiment described in conjunction with FIG. **13**A except that the extra validation process is performed after the calculation of the parameters. In particular, in step **1324**, a threshold value is set in the validator **1208**. If the magnitude of the computer parameters exceeds the threshold, the coefficients for the bin are considered unreliable and the bin is emptied.

In still another embodiment, the filtering step **1326** may be performed before the step **1325**. That is, the calculated parameter values may be averaged with the corresponding current (or, alternatively, a running weighted average of past) predistorter LUT parameters before empty bins are interpolated or extrapolated. Accordingly, averaging only takes place with calculated parameters that have passed the validation process.

FIG. **14** is a block diagram of a DSP module **1400** for implementing a predistorter and trainer, according to one embodiment of the present invention. The DSP module **1400** is substantially similar to the DSP module disclosed in the aforementioned U.S. Pat. No. 5,732,333, but a brief description is included herein for completeness. The DSP module **1400** includes a microprocessor **1401**, a static random access memory (SRAM) **1403** and a nonvolatile memory (NVM) **1405**. In a preferred embodiment, the microprocessor **1401** is a DSP microprocessor TMS320C44 available from Texas Instruments, although any suitable microprocessor can be used. The microprocessor **1401** is connected to the SRAM **1403** and the NVM **1405**. In this embodiment, the NVM **1405** is implemented using a flash electrically programmable read only memory (EPROM). As a result, the DSP module **1400** can be configured or programmed for a variety of functions, such as, for example, forming part of a modulator, interpolator, trainer or predistorter. Further, the DSP module **1400** can be reprogrammed to change its functionality by replacing the configuration program stored in the nonvolatile memory **1405**.

Further, when implementing the predistorter with a DSP module **400**, the predistorter can, on powerdown, store the predistortion values in the nonvolatile memory **405**. As a result, the predistorter can use these stored values immediately after power up to predistort data to be transmitted. Thus, the predistorter does not require a special initialization process with special training sequences as required in many conventional systems.

Additionally, the DSP module in the modulator **403** (FIG. **4**) can be programmed to scale the in-phase and quadrature output signals at start-up and powerdown to "ramp" the input signals to the power amplifier using a look up table (LUT) containing a smooth ramping function of multiplier factors, thereby reducing transients in the power supply voltages and spurious output signal from the power amplifier. In a preferred embodiment, a Gaussian scaling is used. Smooth ramping can be individually applied to individual subcarriers when more than one is transmitted simultaneously.

Further, it has been found that intermodulation products and other distortion (collectively known as "distortion") located in the desired broadcast RF channel (referred to as "in-band") adversely affects the training of the predistorter. The in-band distortion is not only generated by the nonlinearity of the power amplifier, but also from other low frequency sources that are not necessarily from the power amplifier. Sources of these non-power amplifier distortions may include any combination of dynamic power supply effects including ripple and transient noise. In addition, bias irregularities on the power amplifier transistors and thermal transients can introduce low frequency (in-band) effects that are not a reproducible part of the distortion and which is not helpful to model and predistort.

Further, the low frequency distortions appear close to the center of the band when upconverted to the power amplifier output frequency. If these distortions are not due to the power amplifier, then modeling of these distortions and applying their inverses to the power amplifier will not necessarily help. Thus, in an alternative embodiment, the present invention solves this problem by removing the in-band distortion from the power amplifier output signal that is used by the trainer.

Specifically, turning now to FIG. **15**, a block diagram of an alternative embodiment of the present invention is shown. The block diagram is similar to that shown in the preferred embodiment except for additional components adapted to remove the in-band distortion from the power amplifier output. The transmitter **1000** includes a power

amplifier **1002**, a downconverter/demodulator **1004**, an upconverter/modulator **1006**, a trainer **1008**, a predistorter **1010**, a low-pass filter (LPF) **1012**, first summer **1016** and second summer **1014**, broadcast antenna **1024**, and directional coupler **1026**.

In operation, the modulated input is provided to the predistorter **1010**. The predistorter is preferably comprised of an address generator **1018**, a look up table **1020**, and a non-linear predistortion filter **1022**. These elements of the predistorter **1010** are detailed above. The modulated input is a digital complex baseband signal including in-phase (I) and quadrature (Q) components. The predistorter **1010** is operative to filter the modulated input so as to "predistort" the modulated input. The output of the predistorter **1010** is provided to the upconverter/modulator **1006**. The function of the upconverter/modulator **1006** is twofold. First, the upconverter/modulator **1006** acts to combine the in-phase (I) and quadrature (Q) components of the predistorter output. Second, the upconverter/modulator **1006** acts to increase the frequency of the signal to the desired broadcast RF channel. Further, the upconverter **1006** also includes a digital to analog converter for converting the digital signal output by predistorter **1010** into an analog signal for transmission. The output of the upconverter **1006** is then provided to power amplifier **1002** for amplification and broadcast by broadcast antenna **1024**.

Directional coupler **1026** monitors the output of the power amplifier **1002** by monitoring the signal transmitted by broadcast antenna **1024**. The output of the power amplifier **1002** is then input into downconverter/demodulator **1004**. The downconverter/demodulator **1004** performs exactly the opposite function as the upconverter/modulator **1006**. Namely, the downconverter/demodulator **1004** acts to first decrease the frequency of the received signal from the desired broadcast RF channel. It is important that upconverter/modulator **1006** and downconverter/demodulator **1004** be precisely matched to each other in terms of frequency conversion. In other words, the frequency of the output of the downconverter/demodulator **1004** should be substantially the same as the frequency of the input of the upconverter/modulator **1006**.

Next, the downconverter/demodulator **1004** also includes an analog to digital converter for converting the analog received signal into a digital signal. Finally, the downconverter/demodulator **1004** acts to demodulate the digital signal into a digital complex baseband signal having in-phase (I) and quadrature (Q) components.

The output of the downconverter/demodulator **1004** is then provided as an input to the first summer **1016** and the second summer **1014**. Another input of the first summer **1016** is the modulated input. First summer **1016** is operative to subtract the output of downconverter/demodulator **1004** from the modulated input to form an error signal. Because the output of the downconverter/demodulator **1004** (derived from the output of the power amplifier **1002**) is subtracted from the modulated input, the error signal is the negative of the distortion caused by the power amplifier **1002**.

The error signal is provided to LPF **1012**. In the preferred embodiment, LPF **1012** has a cutoff frequency of 24 kHz. However, it can be appreciated by those skilled in the art that the cutoff frequency may be adjusted depending upon the bandwidth of the desired broadcast RF channel. The function of LPF **1012** is to remove that part of the error signal that is outside of the desired broadcast RF channel (referred to as "out-of-band"). The output of LPF **1012** is referred to as the in-band error signal. The in-band error signal is the negative of the in-band distortion caused by power amplifier **1002**.

Next, the in-band error signal is added to the output of the downconverter/demodulator **1004** at second summer **1014**. This has the effect of subtracting the in-band distortion from the output of the downconverter/demodulator **1004**. The output of the second summer **1014** is referred to as the modified power amplifier output signal. The modified power amplifier output signal is then used by the trainer **1008** (as discussed above) to calculate the values stored in look up table **1020** of predistorter **1010**. Thus, the modified power amplifier output replaces the power amplifier output shown in FIG. **6**.

Further, as in the preferred embodiment, the modulated input is provided directly as an input to trainer **1008**. Also as in the preferred embodiment, the trainer has a third input that is the input signal to the power amplifier **1002**. Thus, the trainer **1008** has three inputs: the modified power amplifier output signal, the modulated input, and the input to the power amplifier. Each of these three inputs are acted upon by the trainer **1008** in accordance with the description above to generate numeric values that provided to look up table **1020** for use by the predistorter **1010**.

The embodiments of the predistortion system described above are illustrative of the principles of the present invention and are not intended to limit the invention to the particular embodiments described. Accordingly, while the preferred embodiment of the invention has been illustrated and described, it will be appreciated that in light of the present disclosure, various changes can be made to the described embodiments without departing from the spirit and scope of the invention.

What is claimed is:

1. A method for compensating for distortion caused by a power amplifier in a radio frequency (RF) transmitter, the method comprising:

obtaining an output signal sample that depends on an output signal of the power amplifier,

calculating predictor variables from said output signal sample, said predictor variables being orthogonal to each other;

obtaining an input signal sample that depends on an input signal to the power amplifier;

determining a complex predistortion gain by forming a filter block model, wherein the filter block model receives said predictor variables and outputs the input signal sample, wherein said complex predistortion gain is a function of a complex gain of the filter block model; and

applying said complex predistortion gain to a modulation signal sample to obtain a predistorted signal sample, wherein said complex predistortion gain compensates for distortion caused by the power amplifier when said power amplifier amplifies the input signal, the input signal being dependent on said predistorted signal sample.

2. The method of claim **1** wherein said input signal sample depends on a prior modulation signal sample previously processed by the RF transmitter, said prior modulation signal sample and said modulation signal sample each having an instantaneous power within a predetermined range.

3. The method of claim **2** further comprising forming a table of complex predistortion filter coefficients indexed by predetermined ranges of modulation signal sample instantaneous power.

4. The method of claim **1** wherein said input signal sample depends on a prior modulation signal sample previously

processed by the RF transmitter, said prior modulation signal sample and said modulation signal sample each having a magnitude within a predetermined range.

5. The method of claim **4** further comprising forming a table of complex predistortion filter coefficients indexed by predetermined ranges of modulation signal sample magnitude.

6. The method of claim **1** wherein said output signal sample is obtained by sampling, downconverting and digitizing said output signal of the power amplifier.

7. The method of claim **1** wherein said input signal received by the power amplifier is obtained by interpolating, digital-to-analog converting, and upconverting said predistorted signal sample.

8. The method of claim **1** wherein said complex predistortion gain is a weighted average of both the complex gain of the filter block model and a previous complex predistortion gain.

9. A method for compensating for distortion caused by a power amplifier in a radio frequency (RF) transmitter, the method comprising:

obtaining an output signal sample that depends on an output signal of the power amplifier;

removing the in-band distortion from said output signal sample to form a modified output signal sample;

calculating predictor variables from said modified output signal sample, said predictor variables being orthogonal to each other;

obtaining an input signal sample that depends on an input signal to the power amplifier;

determining a complex predistortion gain by forming a filter block model, wherein the filter block model receives said predictor variables and outputs the input signal sample, wherein said complex predistortion gain is a function of a complex gain of the filter block model; and

applying said complex predistortion gain to a modulation signal sample to obtain a predistorted signal sample, wherein said complex predistortion gain compensates for distortion caused by the power amplifier when said power amplifier amplifies the input signal, said input signal being dependent on said predistorted signal sample.

10. The method of claim **9** wherein said input signal sample depends on a prior modulation signal sample previously processed by the RF transmitter, said prior modulation signal sample and said modulation signal sample each having an instantaneous power within a predetermined range.

11. The method of claim **10** further comprising forming a table of complex predistortion filter coefficients indexed by predetermined ranges of modulation signal sample instantaneous power.

12. The method of claim **9** wherein said input signal sample depends on a prior modulation signal sample previously processed by the RF transmitter, said prior modulation signal sample and said modulation signal sample each having a magnitude within a predetermined range.

13. The method of claim **12** further comprising forming a table of complex predistortion filter coefficients indexed by predetermined ranges of modulation signal sample magnitude.

14. The method of claim **9** wherein said output signal sample is obtained by sampling, downconverting and digitizing said output signal of the power amplifier.

15. The method of claim **9** wherein said input signal received by the power amplifier is obtained by interpolating, digital-to-analog converting, and upconverting said predistorted signal sample.

16. The method of claim **9** wherein said complex predistortion gain is a weighted average of both the complex gain of the filter block model and a previous complex predistortion gain.

17. A system for compensating for distortion caused by a power amplifier in a radio frequency (RF) transmitter, the system comprising:

means for obtaining an output signal sample that depends on an output signal of the power amplifier;

means for removing the in-band distortion from said output signal sample to form a modified output signal sample;

means for calculating predictor variables from said modified output signal sample, said predictor variables being orthogonal to each other;

means for obtaining an input signal sample that depends on an input signal to the power amplifier;

means for determining a complex predistortion gain by forming a filter block model, wherein the filter block model receives said predictor variables and outputs the input signal sample, wherein said complex predistortion gain is a function of a complex gain of the filter block model; and

means for applying said complex predistortion gain to a modulation signal sample to obtain a predistorted signal sample, wherein said complex predistortion gain compensates for distortion caused by the power amplifier when said power amplifier amplifies the input signal, the input signal being dependent on said predistorted signal sample.

18. A system for compensating for distortion caused by a power amplifier in a radio frequency (RF) transmitter, the system comprising:

means for obtaining an output signal sample that depends on an output signal of the power amplifier,

means for calculating predictor variables from said output signal sample, said predictor variables being orthogonal to each other;

means for obtaining an input signal sample that depends on an input signal to the power amplifier;

means for determining a complex predistortion gain by forming a filter block model, wherein the filter block model receives said predictor variables and outputs the input signal sample, wherein said complex predistortion gain is a function of a complex gain of the filter block model; and

means for applying said complex predistortion gain to a modulation signal sample to obtain a predistorted signal sample, wherein said complex predistortion gain compensates for distortion caused by the power amplifier when said power amplifier amplifies the input signal, the input signal being dependent on said predistorted signal sample.

19. A radio frequency (RF) transmitter comprising:

a predistorter coupled to receive a digital data signal;

a digital-to-analog converter coupled to the predistorter;

a power amplifier coupled to the digital-to-analog converter;

an analog-to-digital converter coupled to the output of the power amplifier;

a trainer coupled to the analog-to-digital converter and the predistorter and to receive the digital data signal, wherein the trainer is configured to determine a complex predistortion gain as a function of orthogonal predictor variables and to configure the predistorter with the complex predistorter gain.

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